SimpleCPU_v1a

## Systems and Devices 1 Lec 3b :

 Combinatorial Logic- Block diagram
- ALU : a core requirement of any computer is to process data i.e. the Arithmetic and Logic unit, the ADDER the heart of any CPU.

Binary addition


- Half and full adder
- Basic components can be combined into larger circuits

Demo : relay logic


- Full adder


## Binary addition

- Rjpple adder
- Replicated full adders
Three FA, producing a 3 bit adder
- LSB carry in (CIN) is set to zero
- Carry out (COUT) feeds carry signal to next full adder stage


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Binary addition


## Binary addition

- Rjpple adder
- Add : 7 + 1



Binary addition

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## Binary addition

## Binary addition



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- Rjpple adder
- Add : 7+1


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Binary addition
Ripple adder

- Add : $7+1$

$$
\begin{array}{r}
111 \\
+001 \\
\hline 1000
\end{array}
$$

- Result $8_{10}, 1000_{2}$

- Quick Quizzz
- Convert the following values into binary then confirm the result of the binary addition.
- Is the conversion of the binary result to octal correct?



## Binary addition

## Binary addition

## Binary addition

## - Ripple adder

- MSB Carry Out
- Can be passed to additional full adder stage to allow larger adders to be constructed.
- Can be used to indicate that the result has exceeded the maximum bit representation i.e. an overflow has occurred.
- Important, will use these ideas when writing assembly code.


Ripple adder

- Remember that hardware is not software i.e. each full adder will operate in parallel.
- The result will go through a series of states before it settles down to the final value.



## Binary addition

Ripple adder

- Add : 7+1
- Step 1

> Result $6_{10,}, 0110_{2}$


## Binary addition

- Rjpple adder
- Add : 7 + 1
- Step 2

- Result $4_{10,0100}$



## Binary addition

## Binary addition



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- Quick Quizz
- If each logic gate takes 10 ns to process a signal, what is the critical path delay of this


Example : adder_8.zip


- 8 bit ripple adder

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- Block diagram
- Q : how do we control the ALU's function e.g. pass through, add, subtract and bitwise AND functions, as defined in the instruction set? How do we implement these functions?

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## ALU

- ALU interface and control (CTL) signals
- A(7:0) - 8 bit input, driven by ACC
- $\mathrm{B}(7: 0)$ - 8bit input, driven by Data MUX, IR(7:0) or DIN(7:0)
- CTL(2:0) - 3bit input, function select, driven by control logic
- $\mathrm{Y}(7: 0)$ - 8bit output, result of selected function, $\mathrm{Y}<=\mathrm{A}$ op B .
- Pass through = multiplexer, addition = ripple adder
- How do we perform subtraction and bitwise AND? ©



## Key skills : working in base 2



- Subtract two binary numbers : 150-44
- Positive, integer

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## Key skills : working in base 2

- Borrow case
- Look to the left until the first 1 is found, this defining a block i.e. 10... 0
- Write a 1 in the result and update block to 01.... 1
- Continue subtraction
- Alternatively, another way to think of it
> Borrow '2' from the left column
- Same process you would perform in base 10, but rather than borrowing 10 you borrow 2


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[^0]Key skills : working in base 2


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## Method of Complements

$\stackrel{$| 011 | 010 | 001 | 000 | 111 | 110 | 101 | 100 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| +3 | +2 | +1 | 0 | -1 | -2 | -3 | -4 |$}{\longrightarrow}$

- Q : How do we represent negative numbers?
- Using the complement of a number e.g. 2s complement
- MSB represents the sign: $0=+$ num, $1=-$ num
- Max positive sign bit $=0, \mathrm{MSB}-1$ to $\operatorname{LSB}=1$
- Max negative sign bit $=1, \mathrm{MSB}-1$ to $\mathrm{LSB}=0$
- To convert to a Two's complement representation
- Invert each bit position (one's complement) $0 \rightarrow 1,1 \rightarrow 0$
- Add 1 (carry ignored)


## 2s Complement

| $1_{10}=00000001_{2}$ |  |
| :--- | :--- |
|  |  |
| One's Complement : | 111111110 |
| Add one: | 11111111 |
|  |  |
| $-1_{10}=11111111_{2}$ |  |

$200_{10}=11001000_{2}$
One's Complement : 00110111
Add one : 00111000
$-200_{10}=00111000_{2}$ ???
$100_{10}=01100100_{2}$
One's Complement : 10011011 Add one : 10011100
$-100_{10}=10011100_{2}$

- Examples
- MSB represents the number's sign i.e. a signed number.
- Maximum value that can be represented is halved compared to an unsigned representation


## 2s Complement

| $-100_{10}=10011100_{2}$ |  |
| :--- | :--- |
|  |  |
| One's Complement : 01100011 |  |
| Add one : | 01100100 |
|  |  |
| $100_{10}=01100100_{2}$ |  |

To determine the absolute value of a negative binary number

- Take the Two's complement again
Eight bit signed numbe
$-100_{10}=10011100_{2}$
$100_{10}=01100100_{2}$

Sixteen bit signed number
$-100_{10}=1111111110011100_{2}$
$100_{10}=0000000001100100_{2}$

- Note, when changing the size of a number don't forgot to sign extend.

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Binary subtraction


- Quick Quizzz
- Convert the following values into binary then confirm the result of the binary subtraction.
- Is the conversion of the binary result to hexadecimal correct?
- We could implement the subtraction operation using half and full subtractors, but ...

Key skills : working in base 2


- Using the Two's complement representation simplifies binary subtraction i.e. can be performed using addition
$\Rightarrow A-B=A+(-B)$


## Key skills : working in base 2



- Using the Two's complement representation simplifies binary subtraction i.e. can be performed using addition
$-\mathrm{A}-\mathrm{B}=\mathrm{A}+(-\mathrm{B})$
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Key skills : working in base 2

| 010010110 | 150 |
| ---: | ---: |
| +111010100 | $\underline{-44}$ |
| 11 | - |

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## Addition of negative numbers

- When using Two's complement representation the carry bit can no longer be used to indicate an overflow.
- Oveflow - number (result) can not be represented by the maximum number of bits within a memory location or register i.e. need more bits, can not be stored.
- Overflow is determined by these rules
- If operand sign bits are equal then result sign bit must equal operand sign bit
- E.g. $(A+B)$ or $(-A+-B)$ magnitude always bigger
- If operand sign bit are not equal then overflow can not occur
- E.g. $(A-B)$ or $(-A+B)$ magnitude always smaller


## Addition of negative numbers

| 010010110 <br> +111010100 <br> 1111 | $\frac{150}{40}$ |
| ---: | ---: |
| $\frac{10}{11106}$ |  |

- Different sign bits
- Overflow can not occur

- Matching sign bits
- Overflow may occur
- XOR array


## Adder / Subtractor unit



- How do we perform 2's complement in hardware?
- ADD_SUB_8
- Ripple adder


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- Block diagram
- Q : what else is inside the ALU?

- A : not a lot, a simple ALU for a simple instruction set
- Q : what will happen to the CPD if we have more, "complex" (multiply, divide, square root) instructions? University of York : M Freeman 2021

- Bitwise AND

| A | 00101101 | 45 |
| :--- | :--- | ---: |
| B | $\frac{11000110}{00000100}$ | $\frac{198}{4}$ | or -58



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ALU


- Bitwise AND



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